1 INTRODUCTION

This manual provides maintenance instructions for the 626-PA-6024A plug-in module used with the Series 626 Universal Disturbance Analyzers. Included in this volume are the theory of operation, calibration procedure, and parts lists for the 6024A. Refer to TM-111960G1 Vol. 1 for operating instructions.

2 THEORY OF OPERATION

2.1 General Functional Description

Four microprocessors control the operation of the 6024A. Three on-board CPUs (referred to as the "CPU A", "CPU B", and "CPU C") perform the sampling of the input signals, calculate values for individual frequency components and THD, and determine whether or not a printout is needed. The Mainframe CPU controls the actual printing of disturbances and all other I/O and user-interface functions.

Hardware is divided between two printed circuit cards, the Analog Board and the Digital Board. AC voltages are connected to one end of the Analog Board, which contains input amplifiers, low-pass filters, an analog multiplexer, an Analog-to-Digital converter, and a phase-locked loop. The Digital Board contains the on-board CPUs, 8K-bytes of RAM memory for CPU A, four 8K-byte EPROMS (one for each of the on-board CPUs and one for the Mainframe CPU), interface circuitry for all CPUs, and a communication port for CPU A (for testing only). The two boards are connected by a 24-position jumper cable.

The operation of the 6024A is centered around CPU A. CPU A has control over the input gain switches, analog multiplexer, and A/D converter on the Analog Board, and can communicate with CPU B, CPU C, and the Mainframe CPU. Voltage samples are read from the A/D converter by CPU A and passed to CPUs B and C. Calculations are performed by all three on-board processors; CPUs A, B, and C handle the calculations for Phases A, B, and C, respectively. Values from CPUs B and C are passed back to CPU A for analysis. If there is the need for a printout, CPU A will pass the information to the Mainframe CPU.

The sampling period is phase-locked to the AC voltage applied to Phase A. The phase-locked loop circuit generates a clock which is used to signal CPU A when to read the A/D converter, and is also used to control the low-pass filter cut-off frequency.

2.2 Detailed Description: Analog Board

A Note About Component References

Since this is a three channel plug-in, many of the circuits are repeated three times. The letter "X" in a component designation means that the discussion applies to the corresponding component in all three channels: "R10X" indicates R10A, R10B, and/or R10C. Pin numbers of individual ICs will be indicated by a hyphen and the pin number following the component designation: "U31A-6" means "pin 6 of U31A".

2.2.1 Input Amplifiers

The input voltage is attenuated by a high impedance differential amplifier (op-amp U31X and associated components) with a gain of 1/134. R2X is the common-mode rejection trimmer. The circuitry can tolerate a maximum peak input voltage of about 1400V, corresponding to a maximum of 700V RMS with a crest factor of 2.

A variable-gain amplifer (comprised of op-amp U28X, switches U30X, and associated components) provides three ranges of operation, corresponding to full-scale input voltages of 200, 400, and 600V RMS. A crest factor of up to 2 is allowed in all ranges. The range is selected automatically under control of CPU A based on samples read from the A/D converter; there is no provision for manually selecting one range. Control signals FCHX1, FCHX2, and FCHX3 are set by CPU A to select a range as follows:

FCHX3	FCHX2	FCHX1	NOM. RANGE F.S.	GAIN, U31X-6 TO U28X-6
HIGH	HIGH	LOW	200V RMS (400V PEAK)	1.0
HIGH	LOW	HIGH	400V RMS (800V PEAK)	0.5
LOW	HIGH	HIGH	800V RMS (1200V PEAK)	0.25

2.2.2 Low-Pass Filters

For each of the three channels, two switched-capacitor ICs (U26X and U27X) are cascaded. Each filter IC contains two second-order filters, so that the resulting filter is eighth-order. The cut-off frequency is approximately equal to 1/50 of the frequency of the clock applied to pins 10 and 11 of the filter ICs. This clock is generated by the phase-locked loop, so that the filter cut-off frequency will change as the fundamental frequency changes. As long as the fundamental frequency is between 47 and 63 Hz, the filters will cut off just below the 16th harmonic. C53X and R19X remove any DC offset in the circuit up to that point.

2.2.3 Phase-Locked Loop

The phase-locked loop generates the timing signals which determine the low-pass filter cut-off frequency as well as the sampling rate for measurements. U13 is a phase-locked loop IC, containing a voltage-controlled oscillator (VCO) and a phase detector. The phase detector provides two inputs, one for a reference frequency (pin 2) and one for a synthesized frequency (pin 16). The output of the phase detector (pin 10) is a voltage corresponding to the error of the synthesized frequency as compared with the reference. The error signal is filtered and applied to the VCO control input, so that the VCO is adjusted to match the sythesized frequency with the reference. There are two VCO outputs from U13, a main output (pin 5) and a quadrature output (pin 15) which is 90 degrees out of phase with the main output.

The frequency reference is derived from the input to Phase A. The output from filter U26A is passed through another filter (U25) which cuts off past the fourth harmonic. This signal is converted to digital logic levels (U15-1) and applied through C24 to the phase detector signal input (U13-2). The rising edge of the reference is also used to trigger a one-shot (U8) which in turn causes a sample-and-hold circuit (U9) to sample the phase detector output. It is actually the output of the sample-and-hold which is applied to the VCO control input. This is done to prevent a sudden change in the VCO output

2.2.3 Phase-Locked Loop (continued)

frequency due to a loss of the reference signal. If the reference is lost the sample-and-hold will slowly drift, causing the VCO output to also drift; before this happens, however, the fact that there is no voltage applied to Phase A will prevent the plug-in from making measurements.

The VCO output is passed through two counters (U12 and U14), resulting in a frequency division of 384. This frequency-divided signal is level shifted using Q1 and applied to the phase detector input (U13-16). Thus, the VCO output frequency is 384 times that of the reference. This frequency is half that needed to operate the filters; an exclusive-OR gate (U22) combines the normal and quadrature outputs of the phase-locked loop to produce the proper frequency for the filters.

R23 is the VCO center frequency adjustment, which determines the locking and tracking range of the phase-locked loop. The procedure for adjustment is described in the test procedure.

2.2.4 Analog Multiplexer

The low-pass filter outputs (with offset removed) are applied to analog switches (U21). CPU A selects which of these switches is closed by writing the appropriate code to latch U18. The selected signal is passed through a programmable-gain amplifier (R44-R48, U20, U10; output at U10-1) and connected to a sample-and-hold circuit (U7).

2.2.5 Analog-to-Digital Converter

The output of the sample-and-hold (U7-7) is gain corrected (U5-1) and applied to the input of the A/D converter (U6). This is a 12-bit converter with an internal reference, and is controlled by CPU A as a memory-mapped peripheral. Pin 28 is the A/D status signal, which goes high while a conversion is in progress (this should be high for no longer than 35 microseconds).

2.2.6 Sampling Control Logic

The sampling rate used for measurements is one-fourth the VCO frequency, or 96 times the fundamental of the AC voltages being measured. CPU A controls the analog multiplexer so that every third sample corresponds to one of the input channels; after 96 samples, all three channels have been sampled 32 times.

Samples are taken over four consecutive AC cycles, after which the sampling logic is disabled while calculations are performed. CPU A enables or disables the sampling logic by writing to latch U18; sampling is enabled while U18-19 is low. While sampling is enabled, the rising edge of U12-13 triggers latch U23, which sets the sample-and-hold (U7) to hold and generates a non-maskable interrupt (NMI) to CPU A. CPU A then starts the A/D converter. After the A/D conversion is complete, pins 4 and 13 of latch U23 are pulsed low, setting the sample-and-hold to sample and removing the NMI.

2.2.7 System Check Signal

During a System Check sequence, pin 2 of latch U17 is brought low, causing analog switches U29X to close. This blocks the signal from the inputs and applies a square wave (derived from the VCO) to the input amplifiers.

2.3 Detailed Description: Digital Board

2.3.1 Interface Between CPU A and the Mainframe CPU

NOTE: From now on, the Mainframe CPU will be referred to as the "6502".

CPU A and the 6502 communicate using a bidirectional parallel port. Four tri-state octal latches (U3, U4, U5, U6) are configured so that each CPU can write to two of them and read from the other two:

LATCH	PURPOSE	DIRECTION
U3	Data transfer	CPU A --> 6502
U4	Status code	CPU A --> 6502
U5	Data trnasfer	6502 --> CPU A
U6	Status code	6502 --> CPU A

In addition to the latches, each CPU can interrupt the other and remove the interrupt from the other. For example, CPU A can cause pin 5 of latch U39 to go low, interrupting the 6502; the 6502 can cause this pin to go high when it responds. Likewise, the 6502 can cause U39-9 to go low to interrupt CPU A.

2.3.2 Inteface between CPU A and CPUs B and C

CPU A, CPU B, and CPU C are connected by a common 8-bit bus (pins 13-20 of all three CPUs) for data transfer. In addition, each of these CPUs can interrupt the others. The outputs of latch U38 determine which CPU is being interrupted: CPU A is interrupted when U38-3 is low, CPU B is interrupted when U38-6 is low, and CPU C is interrupted when U38-11 is low. All three CPUs can write to latch U38. Interrupts are used as handshakes during data transfers, which occur between CPU A and the other two CPUs. CPUs B and C do not communicates with each other and therefore do not interrupt each other.

2.3.3 Support Circuitry for On-Board CPUs

All three on-board CPUs have similar support circuitry, which will be described generically (components corresponding to CPU A, CPU B, and CPU C, respectively, will be referenced within parentheses). A crystal (Y1, Y2, Y3) determines the basic microprocessor timing. An address latch (U16, U14, U11) demultiplexes address information from the address/data bus and provides the low-order byte of the address bus. A decoder (U27, U24, U21) divides the address space to select either an 8K-byte EPROM or an octal transceiver. The tranceiver (U8, U2, U1) provides access to the interrupt control latch U38. Program instructions are stored in the EPROM (U28, U23, U20). NAND gates (U18, U15, U12) are used to generate read-enable and write-enable signals.

2.3.4 Additional Circuitry for CPU A

An 8K-byte memory (U26) is used for accumulation of disturbances until they can be printed. An additional decoder (U29) is used to select various latches and ports on both boards. The serial communication interface (internal to CPU A) is accessable for calibration and troubleshooting purposes by connecting a terminal to J3 using a special cable (see the calibration procedure for details). CPU A can cause a hardware reset of CPUs B and C by bringing one of its I/O lines (U30-8) low.

3 CALIBRATION PROCEDURE

NOTE: Unless otherwise noted, all adjustment trimmers are located on the Analog Board.

3.1 Suggested Equipment

1. AC voltage source: variable voltage 0-600V RMS, variable frequency 47-500 Hz, producing a clean sine-wave, and able to phase-lock to a reference frequency.

2. AC voltage source: variable voltage 0-600V RMS, variable frequency 47-63 Hz, producing a clean sine-wave.

3. A CRT-type computer terminal, set to 9600 baud, 8-bit data word, 2 stop-bits, no parity.

4. Oscilloscope, dual trace, 25 MHz

5. AC voltmeter, measuring up to 600V RMS, 47-500 Hz

6. A cable to connect J3 on the 6024 Digital Board with the terminal. The following diagram applies to most terminals:

```
J3-1 <------------<-DATA-<------------< TERMINAL PIN 2
J3-2 -------------GROUND-------------- TERMINAL PINS 1,7
J3-3 >------------>-DATA->------------> TERMINAL PIN 3
                                    /--> TERMINAL PIN 5
                          connect /---> TERMINAL PIN 6
                          together\---> TERMINAL PIN 8
                                  \--< TERMINAL PIN 20
```

7. Extender Card P/N 110260

3.2 Initial Setup

1. Turn the Mainframe OFF and install Extender Card P/N 110260 in one of the five plug-in slots.

2. Remove the four screws securing the Digital Board to the rest of the plug-in assembly. Insert the card-edge fingers into the extender card and lay the Analog Board down on the bench.

3. Set all trimmers to the center of rotation.

3.3 Common Mode Rejection Adjustment

1. Connect an AC voltage source so that a 120V RMS sine-wave is applied to both the "+" and "-" inputs of all three channels, with respect to the Mainframe case ground.

2. Adjust R2A so that the signal at pin 6 of U31A is at a minimum, no greater than 25 mV p-p. Repeat for Phase B (using R2B, U31B) and Phase C (using R2C, U31C).

3.4 Phase-locked Loop Center Frequency Adjustment

1. Apply a 120V RMS, 55.0 Hz sine-wave to the Phase A input.

2. Adjust R23 so that the DC level at pin 5 of U9 is 5.0 VDC.

3.5 Programming the Gain Correction Factors

To compensate for variations in component tolerances, the 6024A internally adjusts measurement values according to gain correction factors stored in an EEPROM (U4 on the Analog Board). For each of the three channels there are three sets of four factors, one set for each of the three input ranges. For example, there exists a set of four correction factors affecting measurements made on Phase B while the input is between 200 and 400V RMS.

Each correction factor occupies one byte in the EEPROM. The EEPROM is accessed using commands provided by a Monitor program. The Monitor is activated by connecting a terminal to J3 on the Digital Board and typing the letter "M". The Monitor commands allow memory to be examined and changed, and allow the contents of the EEPROM to be transferred to and from RAM. Correction factors are set by transferring the EEPROM contents to RAM, modifying certain RAM locations, and transferring the modified values back to the EEPROM.

The correction factor values are determined by making measurements without correction, calculating gain factors based on differences between measured and actual values, changing the EEPROM, and verifying measurement accuracy. The adjustment range using the corection factors is approximately +/- 6% of the reading with no correction. The detailed procedure is as follows:

1. With the Mainframe OFF and no signal applied to the plug-in inputs, connect a CRT terminal to J3 on the Digital Board. Terminal setup and cable wiring are as described above under Suggested Equipment.

2. Turn the Mainframe ON, wait for the usual printouts, and wait for the 6024A to report "FUND TOO LOW" on all three phases.

3. Type the letter "M" on the terminal. After a few seconds, the message "MON: " should appear. The monitor is now active and ready to accept commands. All examples of Monitor commands will include this prompt to show the proper form as it should appear on the CRT screen. If "<return>" appears in an example, this means that the RETURN or ENTER key must be typed to complete the command.

4. Executing the following Monitor commands will set all correction factors to zero and allow the plug-in to indicate harmonic levels in volts rather than percent:

Command:	Comment:
MON: FD100,D17F,00<return>	Fill 128 bytes of RAM with 00
MON: S	Transfer 128 bytes in RAM to EEPROM

5. Turn the Maunframe OFF.

3.5 Programming the Gain Correction Factors (continued)

6. Connect an AC voltage source so that a 60 Hz sine wave can be applied between the "+" and "-" inputs of all three channels. Turn the Mainframe ON and set it to the OPERATE mode. The AC source will be used to provide a known voltage, and the DATA key on the Mainframe front panel wil be used to obtain readings from the plug-in.

7. Set the AC source to 150.0 volts, press the DATA key, and record the values for fundamental voltage for all three plug-in channels. Repeat with the AC source set to 300.0 and 600.0 volts. Fill in Chart 1 with the values. Turn off the voltage source. Press "M" on the terminal to re-enter the 6024 Monitor.

8. Using the data from Chart 1, calculate nine correction factors according to Formula 1 and enter them in Chart 1. For example, suppose Phase A indicates 155.6 V with 150.0 V actual input. The correction factor would be computed by subtracting 155.6 from 150.0, dividing by 150.0, and multiplying by 2048, yielding a decimal value of -76.4. Rounding to -76 and converting to two's-complement hexadecimal, the correction factor value would be B4.

9. Using the correction factors computed in step 8, fill in Chart 2. Each entry in Chart 1 corresponds to one line of entries in Chart 2 so that each correction factor is actually used four times. The 150V, 300V, and 600V entries from Chart 1 correspond to 200V, 400V, and 600V FS entries in Chart 2, respectively.

10. Charts 2 and 3 now indicate exactly what should be in RAM so that the proper values may be transferred to EEPROM. Perform the following Monitor commands:

Command:	Comment:
MON: MD100<return>	Modify RAM starting at address D100
.	For each address shown by the Monitor,
.	type in the value that should be at
.	that address according to Charts 2
.	and 3. Leave the volts/percent
<return>	control set to 00 for now.
MON: S	Transfer 128 bytes in RAM to EEPROM

11. Turn the Mainframe OFF. To verify measurement accuracy, it will be necessary to apply signals to the plug-in inputs containing known levels of fundamental and harmonics. This can be done in at least two different ways: 1) apply fundamental signals to the "+" inputs and harmonic signals to the "-" inputs, or 2) create one signal containing fundamental and harmonics. The first method takes advantage of the plug-ins differential input configuration and allows direct verification of input levels using an AC voltmeter. The second method is closer to "real world" conditions but may be more difficult to verify. Whichever method is chosen, set up the AC voltage sources so that known signals are applied as indicated in Chart 4.

3.5 Programming the Gain Correction Factors (continued)

12. Turn the Mainframe ON, set it to the OPERATE mode, and fill in Chart 4 by using the DATA key to generate present values. Verify that the fundamental and harmonic readings are accurate according to the specifications in the Operating Manual. The fundamental readings should be very close to the actual level, since the correction factors used so far are based on fundamental readings. If one or more of the harmonic readings are inaccurate, it will be necessary to use to Monitor to set the corresponding correction factor to zero, take the appropriate measurement, and recalculate a factor based on the individual harmonic. Chart 2 indicates the exact address in RAM that should be affected; update Chart 2 with recalculated correction factors.

13. After accuracy has been verified, turn off the voltage source(s), re-enter the 6024 Monitor, and execute the following commands:

Command:	Comment:
MON: MD12A<return>	Modify RAM starting at address D12A
D12A 00 FF<return>	Set the volts/percent control to %.
MON: S	Transfer 128 bytes in RAM to EEPROM
MON: W	Transfer 128 bytes in EEPROM to RAM
MON: DD100,D17F	Displays contents of RAM at D100-D17F.

Verify that all data corresponds to Charts 2 and 3. All other locations should be zero except for D17F, which should be equal to the sum of all bytes from D100 through D17E, ignoring overflow.

Chart 1. Uncalibrated Fundamental Values and Correction Factors

ACTUAL VOLTAGE	PHASE A	PHASE B	PHASE C	
150.0V RMS, 60 HZ				
	( )	( )	( )	<-- (correction)
300.0V RMS, 60 HZ				
	( )	( )	( )	<-- (correction)
600.0V RMS, 60 HZ				
	( )	( )	( )	<-- (correction)

Formula 1: $$\text{CORRECTION FACTOR} = \frac{(\text{ACTUAL VOLTAGE} - \text{READING}) \times 2048}{\text{READING}}$$

NOTE: Correction factors in EEPROM exist as two's complement bytes ranging from -128 to +127 (decimal) or FF to 7F (hex).

Chart 2. Correction Factors in RAM (using data from Chart 1)

ADDRESS	FUND+2nd	3rd+4th	5th+6th	7th	
D100 - D103					A, 200V FS
D104 - D107					A, 400V FS
D108 - D10B					A, 600V FS
D10C - D10F					B, 200V FS
D110 - D113					B, 400V FS
D114 - D117					B, 600V FS
D118 - D11B					C, 200V FS
D11C - D11F					C, 400V FS
D120 - D123					C, 600V FS

Chart 3. Preset limits and volts/percent control in RAM

D124:	Ph A THD high limit preset, set to 05
D125:	Ph A THD sensitivity preset, set to 05
D126:	Ph B THD high limit preset. set to 05
D127	Ph B THD sensitivity preset, set to 05
D128	Ph C THD high limit preset, set to 05
D129	Ph C THD sensitivity preset, set to 05
D12A:	Volts/percent control. If 00, present values for harmonics will be in volts (printout still shows "%")

Chart 4. Post-Calibration Verification

FUNDAMENTAL	HARMONIC	PHASE A	PHASE B	PHASE C
150.0V RMS, 60 Hz	50.0V RMS, 120 Hz			
	50.0V RMS, 180 Hz			
MEASURED:	50.0V RMS, 240 Hz			
	50.0V RMS, 300 Hz			
	50.0V RMS, 360 Hz			
	50.0V RMS, 420 Hz			
300.0V RMS, 60 Hz	100.0V RMS, 120 Hz			
	100.0V RMS, 180 Hz			
MEASURED:	100.0V RMS, 240 Hz			
	100.0V RMS, 300 Hz			
	100.0V RMS, 360 Hz			
	100.0V RMS, 420 Hz			
600.0V RMS, 60 Hz	200.0V RMS, 120 Hz			
	200.0V RMS, 180 Hz			
MEASURED:	200.0V RMS, 240 Hz			
	200.0V RMS, 300 Hz			
	200.0V RMS, 360 Hz			
	200.0V RMS, 420 Hz			

PRELIMINARY

626-PA-6030 3-PHASE GRAPHIC A.C. MONITOR

1. INTRODUCTION

This manual provides maintenence instructions for the 626-PA-6030 3-Phase Graphic A.C. Monitor plug-in (hereinafter referred to as the 6030) for use in the Model 626 Universal Disturbance Analyzer. Included in this volume are the theory of operation, maintenance, and parts list for the 6030. For operating instructions refer to the corresponding Volume 1 manual.

2. THEORY OF OPERATION

The 6030 is designed to monitor up to three phases of A.C. power lines and provide disturbance data in both text and graphical form.

The 6030 consists of three circuit boards which occupy two plug-in slots int the 626 mainframe. One board contains the three channels of analog circuitry that is used for the text information. Another board consists of three channels of sampling circuitry for obtaining the graphics data, and a third board oversees the control and interfacing tasks. These three boards will be referred to as the Analog, Graphics, and Digital boards, respectively.

The A.C. signal is fed into the Analog and Graphics boards simultaneously. The Analog board contains circuitry to obtain information on the time average and peak values of the A.C. waveform. This data is made available the Digital board where the values are compared to the user set thresholds. If a theshold is exceeded the information is put on the main CPU stack. Also at this time the Graphics board is signaled that an event has occurred. The Graphics board is continually sampling the incoming A.C. waveform and storing those samples in its own memory. When it is signaled by the Digital board that an event has occured the Graphics board then sets aside the samples containing the cycle in which the event was detected and the samples for one cycle either side of this.

When the event is printed out, the text information is first

printed, followed by the graphical data. There is limited memory available for storage of graphic data. Once all of the available memory is used, no more graphics data is stored until sufficient memory is free. If this occurs, events will still be printed out, but in text only.

3 BLOCK DIAGRAM

3.1 Graphics Board

The applied signal first passes through a wideband attenuator to reduce the signal to more practical levels for measuring. This signal is then applied to two peak detectors, one responding to positive going signals and the other for negative going signals. Every 128 microseconds the output of the peak detectors are read and then reset. The use of peak detectors in the sampling circuitry enables the detection of transients that would otherwise be missed at this sampling rate. The signals from the peak detectors are fed to analog to digital convertors which are read by the CPU and stored for possible later use. All of the timing and control signals for the peak detectors and A/D conversion as well as the required memory and interface signals are controlled by the onboard CPU.

Two bidirectional eight bit ports are used for communication between the Graphics and Digital boards and the mainframe processor. One of these ports is used exclusively for communication between the Graphics and Digital boards during interrupt service.

3.2 Analog Board 6009

3.3 Digital Board 6009

4 DETAILED CIRCUIT DESCRIPTION

4.1 Graphics Board

Wideband input attenuators (RN1,2,C1-4) reduce the input signal to levels more appropriate for use with the remaining circuitry. Diodes CR1-4 clamp the attenuated input to +/- 7.5 Vdc to prevent overdriving the inputs of the operational amplifier and the degradation of its common mode rejection ratio. Op amps U1,2 form a differential amplifier where pots R8, R11 are used to adjust the common mode rejection ratio and gain, respectively. The output of this amplifier feeds another op amp that in conjunction with the analog switch (U2,3) provides a selectable gain of 1,2 or 4 from which the input ranges of 1000, 500, or 250 volts peak are derived. This signal is then fed into two peak detectors (U4,5), one responding to positive peaks and the other to negative peaks. The peak detectors are reset at approximately an eight kilohertz rate by analog switch, U3. Potentiometers U20,25 are used to set up a 2.5 VDC offset which is summed with the peak detector outputs to feed the

single supply analog to digital convertors (U8,9). The 5.0 Vdc reference for the A/D convertors is available at U21-1.

A one shot (U11) provides the reset pulse for the peak detectors when gated with U19. This reset pulse occurs coincident with the reading of the A/D convertors. The time between samples, approximately 128 us, is controlled by the CPU (U6). Samples are stored in RAM (U16,17) on a cycle by cycle basis. The memory has a twelve cycle capacity which is continually being rewritten. A new cycle is started at every sync pulse (U6-20). This pulse is derived from a similar pulse originating on the Analog board.

Two bidirectional ports are provided for communication (U26-29). Of these two ports, one (U26,27) is used for communication between the Graphics and Digital boards during the interrupt service routine. The other port is used for general communications and data transfer between the Graphics board, the mainframe processor and the digital board.

At the end of every cycle the 6303 processor(U6) writes a code into U27 that is read by the mainframe processor. If an event has occurred this code will be echoed back via U26. This signals the Graphics board to save that particular cycle of data and one cycle before and after. Just before the event is printed these samples are transferred to a different RAM (U36). This frees up to three cycles of memory which can then be used to store additional events.

If events occur rapidly enough, the twelve cycles of memory will all be full of data. When this happens the sampling system shuts down and waits until three cycles of memory are free. Once this amount of memory is free sampling will resume.

4.2 Analog Board 6009

4.3 Digital Board 6009

5 MAINTENENCE and CALIBRATION

Calibration Procedure
626-PA-6030 Graphics Board

1. Install 6030 on two plug-in extender cards, P/N 110260.

2. Select 250 Vpk graph range.

3. Apply a 150 Vrms, 60 Hz sinusoidal waveform between the [illegible] input and ground. (Use a signal generator, power amplifier combination whose distortion does not exceed 1%.)

4. Adjust R11X (X refers to A,B,and C) for a reading of 1.5 Vrms +/- 0.5% at U4-1.

5. Turn off signal source.

6. Apply a 150 Vrms, 60 Hz signal from the "+" input to ground.

7. Adjust R8X for a reading of 1.5 Vrms +/- 0.5% at U4-1.

8. Check the voltage at U5-1. It should read 1.5 Vrms +/- 2.5%.

9. Turn off signal source.

10. Adjust R20X for a reading of 2.5 Vdc +/- 0.5% at U4-1.

11. Adjust R25X for a reading of 2.5 Vdc +/- 0.5% at U5-1.

12. Adjust R32 for a reading of 5.00 Vdc.

NOTE: Use a Fluke model 8840A with true rms option or equivalent for all measurements.

Rev. B 5/8/86

5.2 Analog Board 6009

5.3 Digital Board 6009

VOLUME 2
SERVICE MANUAL

PRELIMINARY

MODEL 626GP GRAPHICS PRINTER

SECTION IV
THEORY OF OPERATION

PRELIMINARY

4.1 SCOPE

This volume provides the maintenance instructions for the Model 626 Graphics Printer. It's divided into four sections: (IV) THEORY OF OPERATION, (V) CALIBRATION, (VI) REPLACEABLE PARTS LIST, AND (VII) SCHEMATICS AND GENERAL ASSEMBLY. See Volume 1 for the instalation and operation instructions.

4.2 GENERAL FUNCTIONAL DESCRIPTION

The 626GP consists of two major sections, each described below:

PRINTER CIRCUIT. The printer circuit provides control of printer operations, and serial communications.

POWER SUPPLY CIRCUIT. The power supply circuit provides the necessary operating voltage's for the processor board, and printer.

4.2.1 PRINTER CIRCUIT

A block diagram of the printer circuit is shown in figure 1, the schematic diagram of this circuit appears in schematic 113030-G1. The printer circuit consists of the following functional sections:

1. Processor.
2. Status.
3. Communications.
4. Printer control.
5. Printer

4.3.1 PROCESSOR

The processor consists of a CPU, RAM, EPROM, IRQ control circuit, CPU reset circuit, clock circuit, I/O control circuit, and memory control circuit. The CPU is a generic type 65SC02 CMOS 8 bit microprocessor (U8). The clock circuit consists of 3 hex inverters (U2, 74HCT04), a 10pf capacitor (C1), a 300K ohm resistor (R7), and a 1MHZ crystal (Y1). This circuit provides the necessary CPU, and SYSTEM clock signals. The RAM is an 8Kx8 static CMOS RAM (U11, HM6264) of which 7K is used for input buffering and 1K is used as a CPU scratch pad. The control program is on a 4Kx8 EPROM (U10). The CPU reset circuit consists of an OR gate (U8), a 10K ohm resistor (RN1), and a 6.8uf capacitor (C18), and generates a delayed reset signal which initializes the CPU. The memory control circuit (U7,74HCT32 ; U2,74HCT04) generates the read and write signals required by the memory circuits. The I/O control (U9,74HCT138) provides the device select pulses required. The IRQ control circuit (U1,74HCT00) integrates the IRQ signals from both serial ports and the paper out detection circuit, into a single IRQ signal required by the CPU.

4.3.2 STATUS

The status circuit consists of an input port (U15,74HCT244), printer HOME switch (on printer), paper advance switch (S1), and the paper out detection circuit. This status port monitors the control siginals for serial communications, and printer status. The paper out detection circuit consists of a Photointerrupter, transistors Q1 & Q2, diodes DS1 & DS2 , and resistors R1 to R6. When there is no paper passing through the photointerrupter, the output at E2 goes low turning off transistor Q1 and lighting the red LED (DS1), this turns on transistor Q2 and thus turns off the green LED (DS2).

4.3.3 COMMUNICATIONS

There are two serial ports. One serial port (U18,HD6350 ; U3,1489 ; U4,1488) is configured as a DTE port, and is used to communicate with the 626 mainframe. The other serial port (U12,HD6350 ; U5,1489 ; U6,1488) is configured as a DCE port, and is used to communicate with a terminal.

4.3.4 PRINTER CONTROL

The printer control circuitry consists of two 8 bit parallel driver ports of which one port (U16,UCN4801A) is used to drive the two printer stepper motors and the other port (U17,UCN4801A) drives the head heating elements, and one timer (U13,74121) which is used to adjust the intensity of the dots. The intensity can be set by adjusting R9.

4.3.5 PRINTER

The PRINTER is a thermal printer capable of printing 320Hx8V dots per line. An 8x6 character cell is used.

4.3.6 OPERATIONAL OVERVIEW

On power up the CPU reset circuit provides a delayed reset signal which initializes the CPU. The CPU begins operation by disabling interrupts, and clearing RAM memory. Next the CPU initializes the serial port DCE to 1200 BAUD, 7 bit data, 2 stop bits, even parity, and the serial port DTE to 1200 BAUD, 8 bit data, 2 stop bits, no parity, and enables the receive interrupt. After initializing the serial ports, the CPU initializes the printer by performing a head home sequence. Next the CPU enables the interrupts, and checks to see if data is available from the DCE serial port or if data is available in RAM buffer. Note that the DTE serial port,paper advance, and paper out status are interrupt driven. That is when the DTE serial port receives data, the paper advance switch is pressed, or paper out state is active, an interrupt is generated and the CPU is interrupted to perform a special program and then returns.

Once the CPU determines that there is data available in RAM buffer, it procedes to print the data. The first process is to determine if the data is text or graphics. The following EPSON compatible codes are used:

ESC "G" SET DOUBLE-STRIKE MODE

If the data is text, the CPU fetches from EPROM the pixel information from the FONT table. This table describes the pixel information of a text character in an 8Vx6H character cell. If the data is graphic, the data is already in the required pixel information form. Once the pixel information is available the CPU then sends this information to the printer in the following way. The pixel information is placed in the printer head port U17, and the timer U13 is activated. The CPU then test's to see if the timmer times out by reading the STATUS port U15. Once this process of printing is completed the head position is incremented one place. The CPU checks to see if the head is at the right hand edge of the paper, if so the CPU wraps the line over to the next line.

If the CPU determines that data is available at the DCE serial port, it reads this data and sends it to the 626 via the DTE serial port. If there is an interrupt the CPU determines which device caused the interrupt. If the DTE serial port requested service the CPU reads the data from the serial port and places it in the RAM buffer. Then the CPU checks to see if the bufer is full, if so the CPU disables the serial port. If the interrupt was generated by the paper out sensor the CPU waits for the status to be restored and then returns. If the paper advance switch was pressed the CPU advances the paper until the switch is released.

4.4.1 POWER SUPPLY BOARD

The POWER SUPPLY board is of the switching type, and supplies the necessary operating voltages of +5v, +12v, and -12v. This supply also contains a UPS function using batteries. A block diagram of the power supply is shown in figure 2, the schematic diagram of this assembly appears iin schematic 113036. The power supply consists of the following functional sections:

1) An input filter to suppress conducted EMI.
2) An ON/OFF power switch.
3) A transient suppressor.
4) A +12v switching power supply.
5) A battery charging circuit used for charging the internal battery.
6) A +5.0v converter that supplies a voltage to the printer. This converter enables printer operation while the battery depletes with the 626GP printer running on battery power.
7) A +-12v DC-DC converter.
8) A sense circuit to monitor the power supply voltage VBUS to connect or disconnect the battery.

4.4.2 Line Filter and Transient Suppresion

A line filter, part of AC input connector J2, is used for EMI suppression in conJunction with C46. The filter functions as an attenuator to reduce common mode and normal mode noise to acceptable levels. Varistor R43 clips any voltage transients above 275 volts RMS that manage to pass through the filter.

4.4.3 AC TO DC CONVERSION

An AC input voltage supplied to connector J1 is converted to DC by a circuit whose configuration is determined by selecting 115 or 230 volt Jumpers located on the power supply board, accessible from the P.C. board's edge. (See Assy. 113031). Figure 3 is a simplified diagram of the 115 volt configuration. The primary windings of T4 pins 4 and 3 are connected across the 115 volt input, yielding a secondary voltage of 36 volts RMS center tapped. Bridge rectifier CR27-CR30 and filter capacitors C29 and C30 are connected as a voltage doubler. The unregulated DC voltage developed across C29 and C30 is 2 X 115 X 1.414 or 325 volts.

Figure 4 shows the 230 volt configuration. In this case the primary windings of T4 are connected in series across the 230 volt RMS input. Again, the secondary winding of T4 yields 36 volts RMS center tapped. The bridge rectifier circuit provides a DC voltage of 230 X 1.414, or 325 volts.

Thermistor R42 in the power input circuit helps to limit surge current at power turn-on. As the thermistor is heated, the resistance changes with current and temmperature, and is reduced too a value under 1 ohm. The power dissipation of R42 is thus insignificant with steady state operation of the power supply.

4.4.4 12V SWITCHING POWER SUPPLY

The 36V RMS center-tapped output of transformer T4 is rectified by CR25 and CR26, then filtered by C26. Resistor R59 provides a minimum load. The DC voltage across capacitor C26 powers pulse width modulator (PWM) U2 at pin 15. The PWM's oscillator begins to operate since the common mode voltage at pin 2 is set to 2.5V by R22 and R32. Pulses appear at pins 11 and 14 of U2 at alternate half cycles, turning on transistors Q4 and Q3, respectively. Transistor Q4 turns on Q7 via transformer T2 (pins 3 to 2). During the Q4 off-time, the voltage reversal across the windings of T2 allows current to flow through diode CR15 and winding 1-2 or T2. This prevents the generation of voltage spikes that might damage Q4. A "dead time" between the time Q4 turns off and Q3 turns on prevents transistor overlap.

The operation of Q3 as it drives transistor Q2 via transformer T1 is the same as described for Q4, T2, and Q7. In this fashion, Q7 and Q2 are driven on for each cycle of the pulse width modulator U2. Turn-off of Q7 and Q2 is effected by base-emitter resistors R40 and R15, respectively. Diode CR14 and CR12, respectively, are used to remove charge from the bases.

Capacitors C29 and C30 and transistors Q2 and Q7 are used in a half bridge configuration to drive power transformer T5. (See Figure 5.) Capacitor C28 is included to help prevent transformer T5 from saturating. The DC component of the waveform changes for every half cycle of pulse width modulator U2. When Q2 is on, current flows through C30, C28, T5, and Q2, and the voltage developed across the primary of T5 is referenced to ground. When Q7 is on, current flows through Q7, T5, C28, and C29, and the voltage across the primary of T5 is referenced to the voltage seen by C28 (approximately +Vdc/2). Addition of C28 to the bridge helps prevent saturation of T5 caused by mismatches introduced by Q2 and Q7.

Since transistors Q7 and Q2 drive current through the primary of T5 on alternate pulses, each is provided with an RC snubber circuit to dissipate energy at turn-off. RC networks R39/C27 and R17/C3 are used to charge a capacitor when the associated switching transistor (Q7 and Q2, respectively) is turned off. This enables the primary of T5 to dissipate power in the snubbers, rather than the power transistors, at transistor turn-off. Diodes CR13 and CR11 are used with the snubbers to provide a current path for the primary winding of T5. This allows stored energy in the primary to be circulated by way of a current through diodes CR11, CR13 into capacitors C29, C30 when Q2 and Q7 are not conducting.

The voltages developed across the secondary windings of T5 are rectified and filtered to a DC voltage level by CR16, L4, and C4. The DC output voltage can be adjusted by resistive divider R27, R18, and R26. The voltage at the arm of R18 is monitored by U2-1, the inverting input of the PWM error amplifier. U2-1 and U2-2 compare inputs to determine the proper pulse width set by pulse width modulator U2. Potentiometer R18 is adjusted to produce a +12v output across C4 and set the pulse width. The pulse width will adjust for load variations and line variations seen by this section of the power supply. The DC output (V BUS) developed across C4 is used to power the other converters on the power supply board, as well as charge the unit's battery.

At PWM U2, oscillator components C7 and R21 set the switching frequency to 21 kHZ. Components C5, R20, C6, CR5, R19, CR4 and C9 set the compensation of the error amplifier (Pins 1, 2 and 9). The dead band from the PWM is limited by R19, CR5 and C9 by clamping the error amplifier voltage to prevent pulse overlap.

4.4.5 +5.0V CONVERTER

The +5.0V converter's output is used to drive circuitry for the printer as well as the print head and the printer motor. The +5.0V converter is a flyback switcher. The converter consists of the following sections:

1) A switching regulator and timing capacitor: U3, C43

2) Current limiting resistor: R82

3) A switching pass transistor, Q14, and driving circuitry R83, R88, R84

4) Flyback diode: CR35

5) An output filter: L24, C44, C45

The current limit function is activated by the voltage drop across R82 (U3-14 to U3-13). In order to develop a potential across R82, transistor Q14 must be turned on. Turn-off of Q14 causes peak currents to be detected by R82. The current through R82 provides the needed forward voltage drop from U3-14 to U3-13. When a voltage of approximately 0.45V is sensed at U3-14 to U3-13, the internal circuitry of U3 inhibits the output at pin 10, causing Q14 to turn off. This serves to limit the current delivered to the +5.0V output.

The oscillator on-time of U3 is set by C43. Since the switching regulator changes the off-time of each pulse delivered to output U3-10, the frequency of the output is variable.

← See Rob on missing 2 pages.

4.4.6 INTERNAL BATTERY

The internal battery connection is made to the power supply board via connector J3. The nominal 8.4V, 0.5 Amp-hour Nicad battery is fused by a 3 amp fuse (F2) located on the power supply board. Diode CR7 is used to connect the internal battery to the VBUS voltage by way of relay K1. Relay K1 is used to connect or disconnect the battery from the VBUS voltage.

4.4.7 BATTERY CONNECT/DISCONNECT CIRCUIT

Relay K1 is used to disconnect the battery when: 1) the 626 Graphics Printer power switch is OFF; and 2) when the battery voltage is depleted below 7.7 volts. Otherwise, during normal operation, relay K1 is closed and the battery is connected to VBUS.

The circuit U1, R4, R5, R10, R11, R12, R81, C1 is used to sense the voltage at VBUS to determine when the battery is to be connected or disconnected. Resistor divider R12, R5 set a reference voltage to U1 pin 8. Resistor dividers R10, R4 are used to allow VBUS to be sensed and compared at U1 pin 9. Capacitor C1 is needed so that slitches do not trigger the battery disconnection prematurely. R11 is used to give some hysteressis to comparator U1, so the battery is connected after the voltage at VBUS is higher then the battery voltage during POWER ON.

Transistor Q5 is used to power the relay coil of K1. The base of Q5 is driven by U1-14 but when the power switch is turned OFF, the base of Q5 is grounded, preventing relay K1 from connecting the internal battery to voltage VBUS.

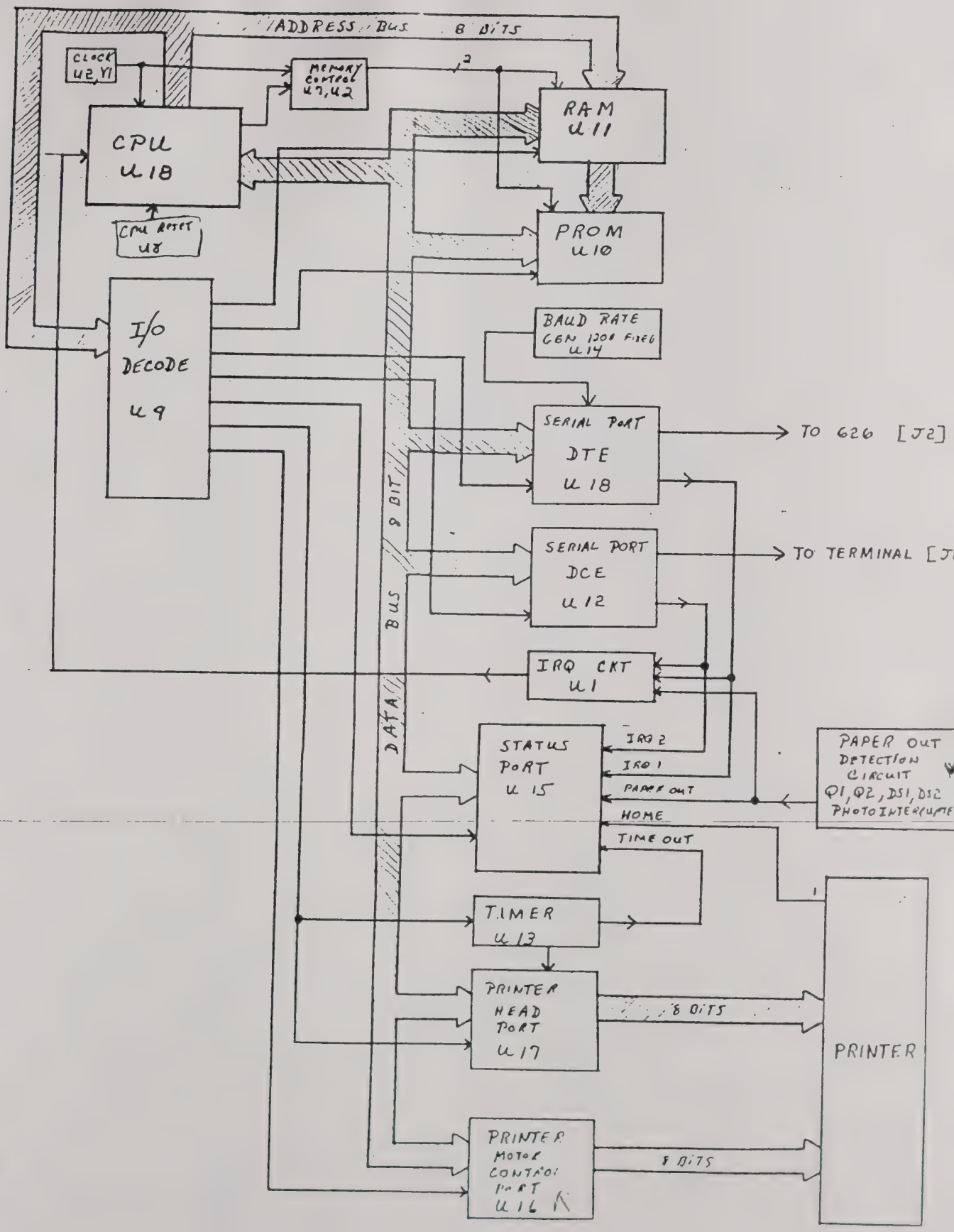

FIGURE 1. CPU BLOCK DIAGRAM

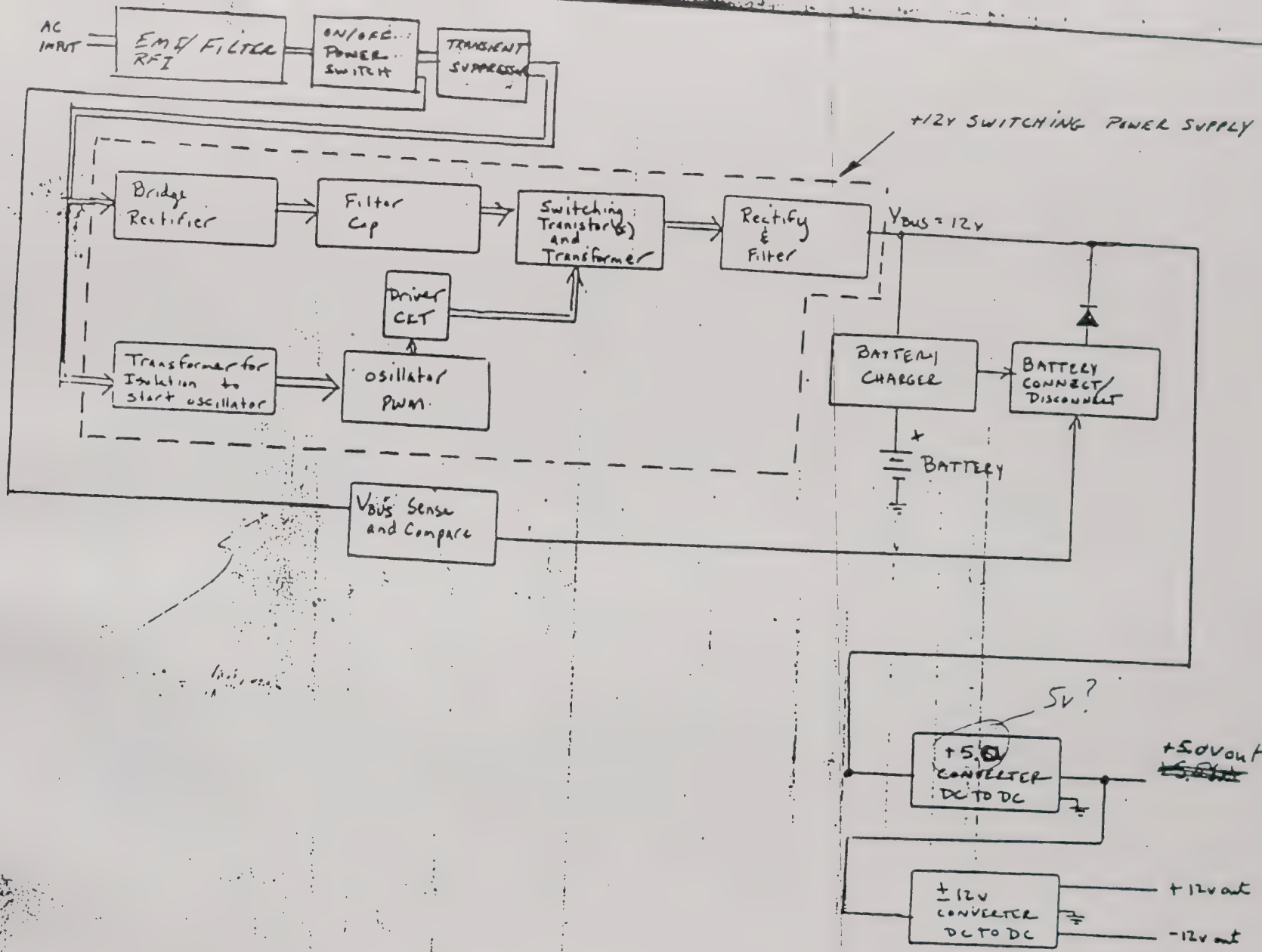

Figure 2: Power Supply Block Diagram

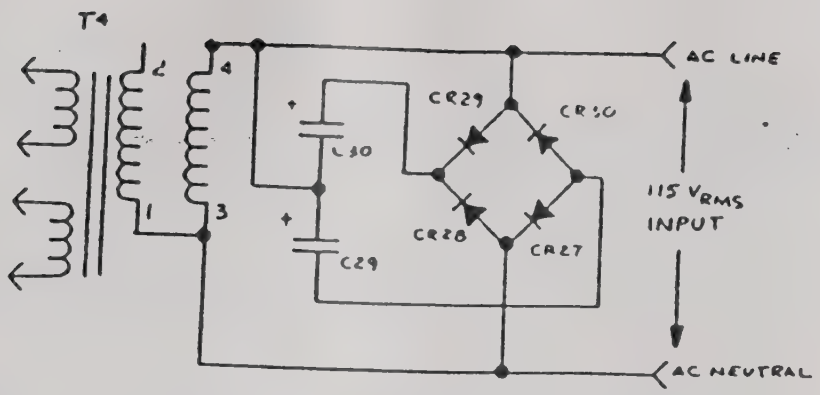

Figure 3. 115V Configuration

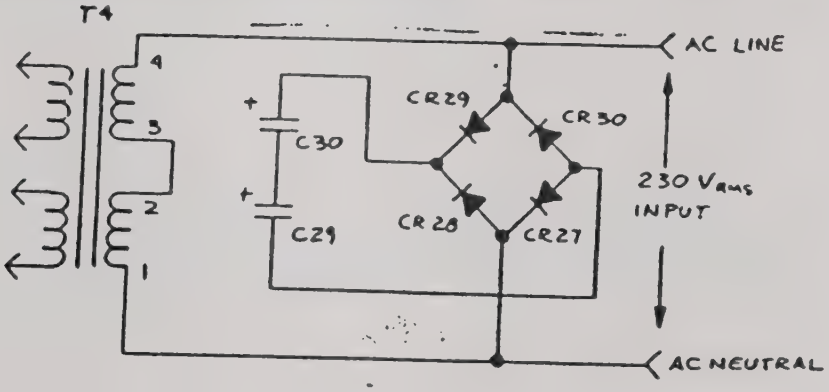

Figure 4. 230V Configuration

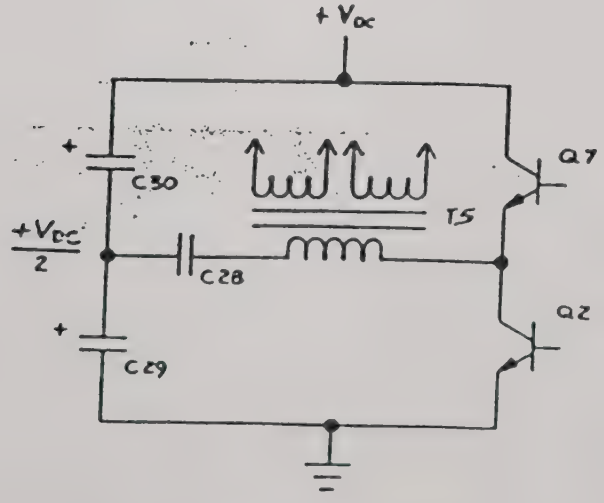

Figure 5. Half Bridge Circuit

SECTION V
CALIBRATION

5.1 CALIBRATION PROCEDURE

With the 626GP powered off, remove the power line, remove the front panel from the plastic case, and unplug the battery connector from the power supply board. Place 626GP face down on work bench, CAUTION power line voltage will be present on the power supply board, reconnect power line and turn on unit. With a DC volt meter measure the voltage across C4 on the power supply board. This voltage should be +12V, adjust potentiometer R18 if necessary. With a DC volt meter measure the voltage at pin #1 on connector J1, this voltage should be +5.0 V, if necessary adjust potentiometer R86 on power supply board.

The printers dot intensity can be adjusted with potentiometer R9 on the CPU board. This potentiometer adjusts the delay on timmer U13. The correct level of intensity is anywhere between gray and black. The suggested delay at timmer U13 pin #1 is 260 usec.

Turn off the 626GP and remave the power line. Replace the unit in its plastic case.

==BATTERY_CAUTION==

DO NOT ATTEMPT TO SERVICE THE 626 GRAPHICS PRINTER WITHOUT FIRST DISCONNECTING THE BATTERY PACK. UNPLUG THE BATTERY CONNECTOR FROM THE POWER SUPPLY BOARD AFTER REMOVING THE 626 GRAPHICS PRINTER'S CHASSIS FROM ITS PLASTIC CASE.

SECTION VI
REPLACEABLE PARTS LIST

6.1 GENERAL

The replacable parts are listed in table 6-1 which besins below. Contained in the parts list is each part's description, identification number, reference designation, and manufacturer's code. Much of the replaceable hardware was omitted from this table. Further information on the replaceable hardware, contact the Dranetz Service Corporation.

6.1.1 Reference Designations

Refer to figures 7-1 through 7-6 in section VII for assembly drawins reference designations of repaceable parts.

Table 6-1. Replaceable Parts List (Page 1 of xx)

PRINTER HARDWARE

REFERENCE DESIGNATION	PART OR IDENT. #	MAN. CODE	DESCRIPTION
	110885-G1		PRINTER
	110886-G1		PHOTOINTERRUPTER
	113016-G1		PAPER SPOOL SHAFT
	110884-G1		BATTERY PACK
S1	104870-G1		SWITCH, SPST, MOMEN.,NO
	113020-G1		KEY, MODIFIED
	17666		115v LINE CORD
	110726		230v LINE CORD
	113003-G1		PRINTER INTERFACE CABLE
	113004-G1		626GP CABLE
	113002-G1		HARNESS
	113022-G1		FLEX CABLE

PRINTER CPU BOARD

REFERENCE DESIGNATION	PART OR IDENT. #	MAN. CODE	DESCRIPTION
USED@U12,18	110749-G7		I.C. SOCKET 24 PIN
USED@U10,11	110749-G8		I.C. SOCKET 28 PIN
USED@U8	110749-G9		I.C. SOCKET 40 PIN
C1	104016-G2		CAP FXD MICA 10pf,+/-5%,500v
C2,C3,C4,	104022-G4		CAP FXD MICA 200pf,+-5%,500v
C5,C10,C11,	"		"
C12,C13	"		"
C6,C9,	103209-G1		CAP FXD CER 0.10uf,+-20%,50v
C14,C15	"		"
C7,C8,C16	103209-G2		CAP FXD CER 0.22uf,+-20%,50v
C17	104080-G1		CAP FXD ELEC 47uf,+-20%,50v
C18	104005-G5		CAP FXD TAN 6.8uf,+-10%,35v
DS1	104976		RED L.E.D. (W/MTG GROMMET)
DS2	104975		GREEN L.E.D. (W/MTG GROMMET)
USED@DS1,2	110835-G3		SPACER 1/4 DIA x 3/16 LG
USED@J1	2275-N120		FLAT WASHER, NYLON
P1	113022-G1		FLEX CABLE
J1	110830-G4		D TYPE FEMALE 25 PIN CONN.
J2	110830-G3		D TYPE MALE 25 PIN CONN.
J3	110887-G1		HEADER,DOUBLE ROW,24 POS.
Q1,Q2	104505		TRANSISTOR 2N3904
R1	108253		RES FXD COMP 430 ,+-5%,1/4W
R2	108255		RES FXD COMP 510 ,+-5%,1/4W
R3	108286		RES FXD COMP 10K ,+-5%,1/4W
R4,R6	108246		RES FXD COMP 220 ,+-5%,1/4W
R5	108289		RES FXD COMP 13K ,+-5%,1/4W
R7	108321		RES FXD COMP 300K,+-5%,1/4W
R8	108269		RES FXD COMP 2K ,+-5%,1/4W
R9	104703-G10		VAR RES COMP 5K ,+-10%,1/2W
RN1	104791		RES NETWORK SIP,10K ,+-10%
U1	112029-G1		IC QUAD 2-INPUT NAND GATE
U2	112029-G2		IC HEX INVERTER
U3,U5	104222-G2		IC QUAD LINE RECEIVER
U4,U6	104222-G1		IC QUAD LINE DRIVER
U7	112029-G3		IC QUAD 2-INPUT OR GATE
U8	104249-G3		IC CMOS CPU
U9	104290-G2		IC DECODER

Prints needed for Power Supply Technical Manu

LM 113031-G1, G2
Assy 113031-G1, G2
Schematic 113036-G1, G2

PRINTER CPU BOARD

LM 113025-G[]
113030-G1 SCHEMATIC
113025-G1 ASSEMBLY
113001-G1 INTERCONNECTING WIRA

MAIN ASSEMBLY 113000-GE]
626 CP CABLE 113004-G[]

MP MASTER
MA23072